## LISTING OF THE CLAIMS:

Claims 1-21 (Cancelled)

Claim 22 (Original) An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material, said silicon-containing semiconductor material being doped with an impurity to provide carriers of holes, electrons or both holes and electrons; and

a first layer of $CoXSi_2$, wherein X is an alloying additive, said alloying additive being present in said first layer in an amount of from about 0.01 to about 50 atomic %,

said first layer and said silicon-containing semiconductor material forming an interface having a predetermined roughness and being substantially free of Co silicide spikes descending into said silicon-containing semiconductor material.

Claim 23 (Original) The electrical contact of Claim 22 wherein said alloying additive is selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

Claim 24 (Original) The electrical contact of Claim 23 wherein said alloying additive is C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir or Pt.

Claim 25 (Original) The electrical contact of Claim 24 wherein said alloying additive is Si, Ti, V, Cl, Ni, Ge, Nb, Rh, Ta, Re or Ir.

Claim 26 (Original) The electrical contact of Claim 22 wherein said alloying additive is present in said first layer in an amount of from about 0.1 to about 20 atomic %.

Claim 27 (Original) An electrical contact to a region of a silicon-containing substrate comprising:

a substrate having an exposed region of a silicon-containing semiconductor material, said silicon-containing semiconductor material being doped with an impurity to provide carriers of holes, electrons or both holes and electrons; and

a first layer of NiXSi, wherein X is an alloying additive, said alloying additive being present in said first layer in an amount of from about 0.01 to about 50 atomic %,

said first layer and said silicon-containing semiconductor material forming an interface having a predetermined roughness and being substantially free of Ni silicide spikes descending into said silicon-containing semiconductor material.

Claim 28 (Original) The electrical contact of Claim 27 wherein said alloy additive is selected from the group consisting of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo,

Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

Claim 29 (Original) The electrical contact of Claim 28 wherein said alloying additive is C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir or Pt.

Claim 30 (Original) The electrical contact of Claim 29 wherein said alloying additive is Si, Ti, V, Cr, Ni, Ge, Nb, Rh, Ta, Re or Ir.

Claim 31 (Original) The electrical contact of Claim 27 wherein said alloying additive is present in said first layer in an amount of from about 0.1 to about 20 atomic %.

Claim 32 (Cancelled)